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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,864	12/17/2001	Aaron K. Martin	884.681US1	2720

7590 10/21/2003

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EXAMINER	
CHOE, HENRY	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 10/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,864	MARTIN ET AL.	
	Examiner	Art Unit	
	Henry K Choe	2817	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,11,12,16,17,19,22-24 and 28* is/are rejected.

7)☒ Claim(s) *3-6,8-10,13-15,18,20,21 and 25-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 2, 11,23 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Cosand (Fig. 4).

Regarding claims 1 and 23, Cosand (Fig. 4) discloses an amplifier circuit comprising a voltage to current converter (Q1, Q2) having a differential input node (IN,

INX) and a differential output node (the collectors of the transistors Q1 and Q2), and a current multiplier (Q15 and Q7; Q16 and Q8) which is coupled to the differential output node (the collectors of the transistors Q1 and Q2) of the voltage to current converter circuit (Q1, Q2).

Rearding claims 2 and 24, the current multiplier (Q15 and Q7; Q16 and Q8) includes an output node (a collector of Q7 and a collector of Q8) and the circuit further includes a load device (R3, R4) which is coupled to the output node (a collector of Q7 and a collector of Q8) of the current multiplier (Q15 and Q7; Q16 and Q8).

Regarding claim 11, Cosand (Fig. 4) discloses an amplifier circuit comprising a differential pair of input transistors (Q1, Q2), a current multiplier (Q15 and Q7; Q16 and Q8), and a pair of load devices (R3 and R4).

Claims 16, 17, 19, 22 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Jett Jr (Fig. 2).

Regarding claim 16, Jett Jr (Fig. 2) discloses an amplifier circuit comprising a current multiplier (10, 11) with a digitally programmable current gain (21).

Regarding claim 17, Jett Jr (Fig. 2) further discloses a voltage to current converter circuit (40, 41) which is coupled to an input side of the current multiplier (10, 11).

Regarding claim 19, the current multiplier (10, 11) in Fig. 2 of Jett Jr includes a plurality of current mirrors (16 and 17; 18, 19) with digitally programmable gain (21).

Regarding claims 22 and 28, the digital programmable gain (21) inherently includes a processor, a processor peripheral, a memory, and a memory controller which is well known in the art.

Claims 1, 7, 11, 12, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by IEEE [Adams et al (Fig. 1)].

Regarding claim 1, IEEE [Adams et al (Fig. 1)] discloses an amplifier circuit comprising a voltage to current converter (Linearized Input Stage) having a differential input node (V1, V2) and a differential output node (I1, I2), and a current multiplier (Programmable Current Mirrors) which is coupled to the differential output node (I1, I2) of the voltage to current converter circuit (Linearized Input Stage).

Regarding claim 7, IEEE [Adams et al (Fig. 1)] further includes the current multiplier (Programmable Current Mirrors) includes a plurality of selectable current source circuits (A2 of left Programmable Current Mirror and A1 of right Programmable Current Mirror) to provide a digitally controlled programmable gain.

Regarding claim 11, IEEE [Adams et al (Fig. 1)] discloses an amplifier circuit comprising a differential pair of input transistors (Linearized Input Stage), a current multiplier (Programmable Current Mirrors), and the IEEE [Adams et al (Fig. 1)] inherently includes a pair of load devices since the Fig. 1 of IEEE (Adams et al) does not work without a load.

Regarding claim 12, the current multiplier (Programmable Current Mirrors) in Fig. 1 of IEEE (Adams et al) includes a plurality of selectable current source circuits (A2 of left Programmable Current Mirror and A1 of right Programmable Current Mirror).

Regarding claim 16, IEEE [Adams et al (Fig. 1)] discloses an amplifier circuit comprising a current multiplier (programmable current mirror) which inherently includes a digitally programmable current gain since it would not work without a digitally programmable current gain.

Regarding claim 17, IEEE [Adams et al (Fig. 1)] further discloses a voltage to current converter circuit (Linearized Input Stage) which is coupled to an input side of the current multiplier (programmable current mirror).

Allowable Subject Matter

Claims 3-6, 8-10, 13-15, 18, 20, 21 and 25-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 3, 8 and 9, the closest prior art of record, Cosand (Fig. 4) does not disclose the following limitations: the current multiplier and the second current multiplier have differential output nodes coupled in common. Regarding claim 13, the closest prior art of record, IEEE [Adams et al (Fig. 1)] does not disclose the following limitations: each of the plurality of selectable current source circuits is configured to be responsive to a digital control signal. Regarding claim 14, the closest prior art of record,

IEEE [Adams et al (Fig. 1)] does not disclose the following limitations: a second current multiplier coupled between the second differential pair of transistors and the pair of load devices. Regarding claim 18, the closest prior art of record, IEEE [Adams et al (Fig. 1)] does not disclose the following limitations: the functional limitations of the processor. the closest prior art of record, IEEE [Adams et al (Fig. 1)] does not disclose the following limitations: Regarding claim 20, the closest prior art of record, IEEE [Adams et al (Fig. 1)] does not disclose the following limitations: a plurality of voltage to current converter circuits. Regarding claim 25, the closest prior art of record, Cosand (Fig. 4) does not disclose the following limitations: the plurality of current multipliers have a programmable current gain.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent numbers (5,455,522; 4,853,610) are the programmable current mirrors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (703) 305-0576.

HENRY CHOE
PRIMARY EXAMINER

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